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Simultaneous DMA and PIO Access in the ISP1161x, ISP1181x and ISP136x Device Controller

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Application Note

Rev. 1.1

Revision History:

Version	Date	Description	Author
1.1	Mar 2003	Added ISP1362	Rajaram Veerappan
1.0	Feb 2003	First version.	Rajaram Veerappan

Note: ISP1161x denotes any Philips USB single-chip Host Controller and Device Controller whose name starts with 'ISP1161'; this includes ISP1161A, ISP1161A1 and any future derivatives. ISP1181x denotes any Philips USB interface device whose name starts with '1SP1181'; this includes ISP1181, ISP1181A, ISP1181B, and any future derivatives. ISP136x denotes any Philips single-chip USB OTG dual-role controller whose name starts with 'ISP136', this includes ISP1362, ISP1363 and. any future derivatives.

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1. Introduction

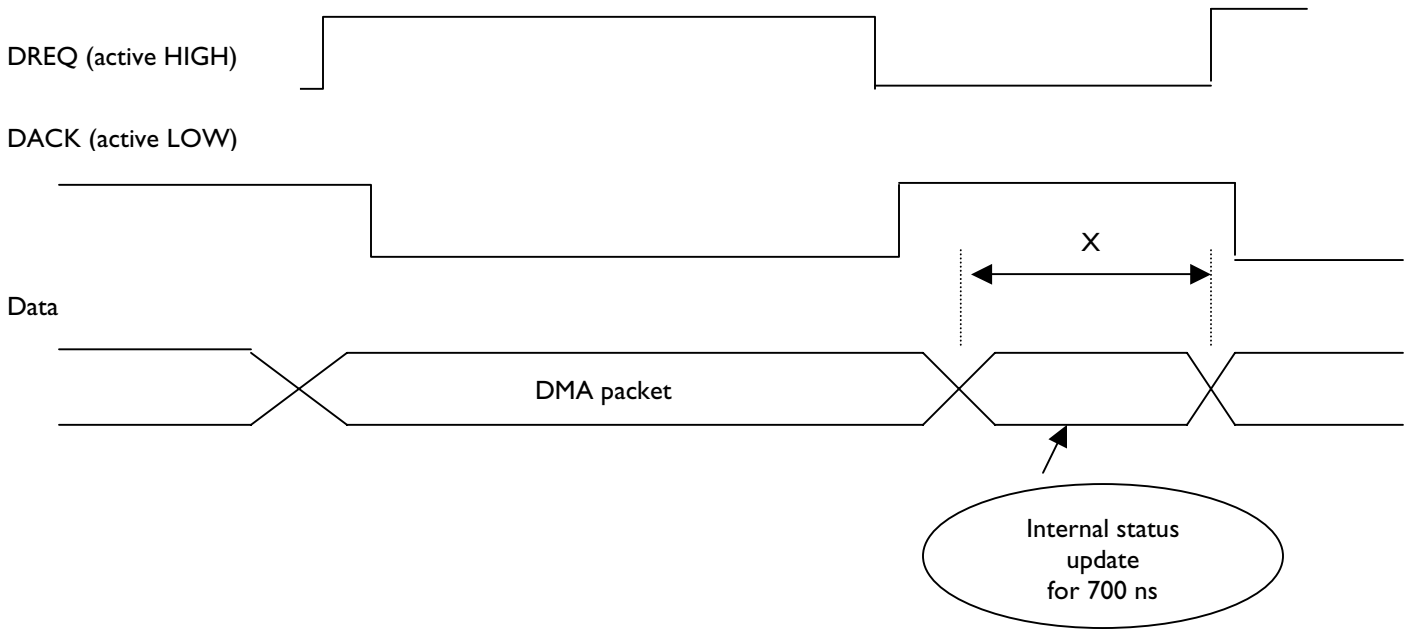
In some complex applications, such as multifunctional adapters, there may be a need to simultaneously perform direct memory access (DMA) and parallel I/O (PIO).

This document explains the points that must be covered while performing simultaneous DMA and PIO accesses in the device controller of the ISP1161x, the ISP1181x, or the ISP136x.

2. Timing constraint

When the Device Controller is performing DMA transfer, it can also perform PIO access in between. You have to ensure, however, that the internal RAM is not disturbed because of this access.

For example, during the DMA transfer for an IN token: While the buffer (IN endpoint) is being filled up, once the packet boundary[1] is reached, internally the DMA state machine updates the RAM status for 700 ns. After every 64 bytes, the state machine updates the status for 700 ns. It is during this time that access to the internal RAM is not recommended. The commands in Section 3 directly affect the RAM; when issued, they lock up the internal RAM. When these commands are issued during the critical period of 700 ns, the internal RAM gets corrupted, leading to data error.



There cannot be any PIO access during this time.

Therefore, during the 'x' period, there cannot be any PIO access to the ISP1161x, ISP1181x or ISP136x Device Controller.

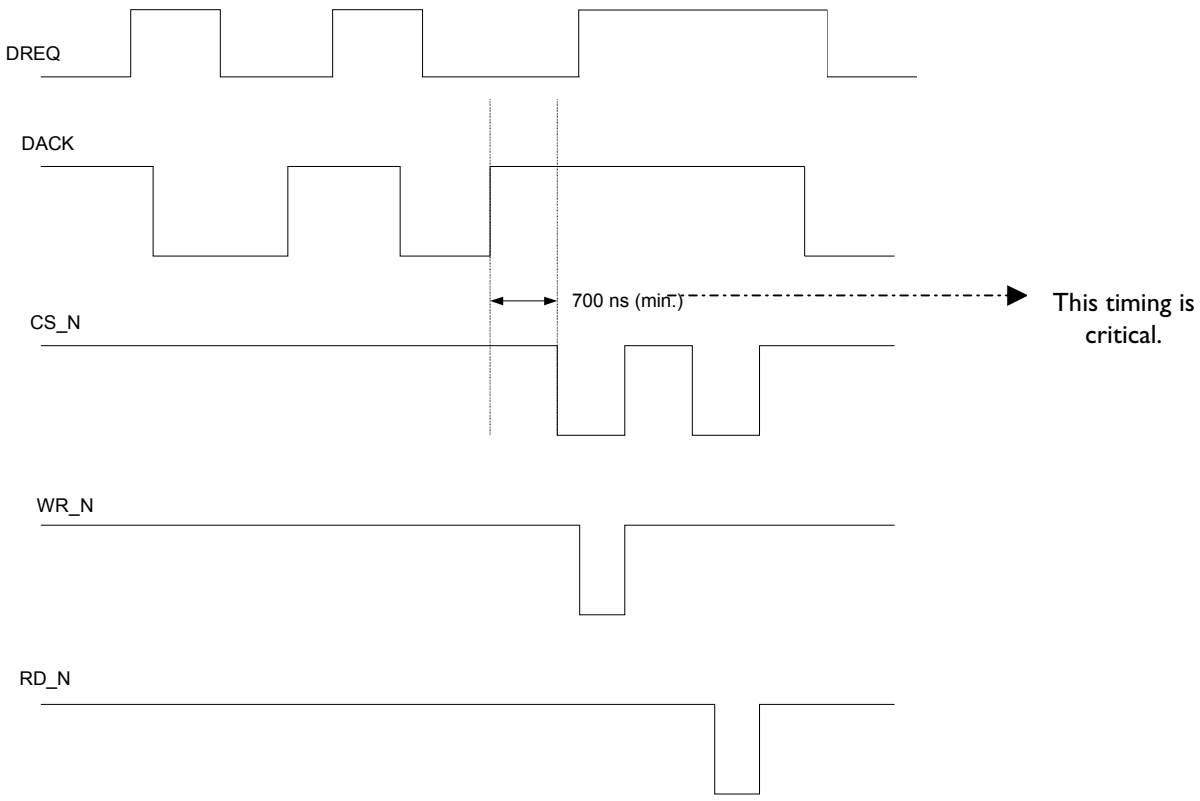
[1] Packet boundary is the endpoint size. If the endpoint size is configured as 64 bytes, then packet boundary is 64 bytes.

3. Command sets

The following commands lock the internal RAM. If the following commands need to be executed during DMA access, then issue the commands 700 ns after the DACK deassertion.

- Stall control OUT/IN endpoint (0x40/0x41)
- Stall endpoint n (0x42 to 0x4F)
- Read control OUT/IN status (0x50/0x51)
- Read endpoint n status (0x52 to 0x5F)
- Validate control OUT/IN buffer (0x60/0x61)
- Validate endpoint n buffer (0x62 to 0x6F)
- Clear control OUT/IN buffer (0x70/0x71)
- Clear endpoint n buffer (0x72 to 0x7F)
- Unstall control OUT/IN endpoint (0x80/0x81)
- Unstall endpoint n (0x82 to 0x8F)
- Acknowledge setup (0xF4)

While issuing these commands, you must observe the timing constraint mentioned in Section 2. The following diagram shows the DMA and PIO accesses:



In the diagram, it is assumed that:

- DREQ is active HIGH,
- DACK is active LOW, and
- RD_N, CS_N and WR_N are active LOW.

If the specified timing constraints are not properly addressed, then the internal RAM could get corrupted, resulting in data error.

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